IN THE CLAIMS:

Please cancel claims 1, 8, 15, and 22 and amend the remaining claims as follows:

1. (Canceled).

2. (Currently Amended) A semiconductor structure formed on a substrate comprising:

a ring oscillator receiving a first voltage and a second voltage as power supplies, wherein said ring oscillator outputs a ring oscillator output; and

an inverter receiving said ring oscillator output as an input, said inverter being coupled to a device under test and said inverter receiving a third voltage and a fourth voltage as power supplies,

wherein current drawn by said inverter provides a measurement of capacitance of said device under test,

~~The structure in claim 1,~~ wherein a difference between said third and fourth voltages is less than or equal to approximately one-third of the difference between said first and second voltages.

3. (Currently Amended) The structure in claim [[1]] 2, wherein a difference between said third and fourth is less than the sum of absolute values of threshold voltages of n-type and p-type field effect transistors that comprise said inverter.

4. (Currently Amended) The structure in claim [[1]] 2, wherein said capacitance comprises:

said current drawn by said inverter divided by a multiplication result of the frequency of said ring oscillator output multiplied by the difference between said third and fourth voltages; less

a capacitance constant for said structure.

5. (Original) The structure in claim 4, wherein said capacitance constant is for said semiconductor structure alone and does not include any part of said capacitance of said device under test.

6. (Currently Amended) The structure in claim [[1]] 2, wherein said measurement of capacitance of said device under test is used to determine the thickness of a gate oxide.

7. (Currently Amended) The structure in claim [[1]] 2, wherein said device under test comprises one of a gate oxide capacitor, a gate conductor, a channel, and an interconnect.

8. (Canceled).

9. (Currently Amended) An on-chip test device comprising:

a ring oscillator receiving a first voltage and a second voltage as power supplies, wherein said ring oscillator outputs a ring oscillator output; and

an inverter receiving said ring oscillator output as an input, said inverter being coupled to a device under test and said inverter receiving a third voltage and a fourth voltage as power supplies,

wherein said on-chip test device and said device under test are located on the same semiconductor chip; and

wherein current drawn by said inverter provides a measurement of capacitance of said device under test,

~~The device in claim 8,~~ wherein a difference between said third and fourth voltages is less than or equal to approximately one-third of the difference between said first and second voltages.

10. (Currently Amended) The device in claim [[8]] 9, wherein a difference between said third and fourth voltages is less than the sum of absolute values of threshold voltages of n-type and p-type field effect transistors that comprise said inverter.

11. (Currently Amended) The device in claim [[8]] 9, wherein said capacitance comprises:

said current drawn by said inverter divided by a multiplication result of the frequency of said ring oscillator output multiplied by the difference between said third and fourth voltages; less

a capacitance constant for said structure

12. (Original) The device in claim 11, wherein said capacitance constant is for said on-chip test device alone and does not include any part of said capacitance of said device under test.

13. (Currently Amended) The device in claim [[8]] 9, wherein said measurement of capacitance of said device under test is used to determine the thickness of a gate oxide.

14. (Original) The device in claim [[8]] 9, wherein said device under test comprises one of a gate oxide capacitor, a gate conductor, a channel, and an interconnect.

15. (Canceled).

16. (Currently Amended) A semiconductor structure formed on a substrate comprising:

a ring oscillator receiving a first voltage and a second voltage as power supplies, wherein said ring oscillator outputs a ring oscillator output; and

a plurality of inverters receiving said ring oscillator output as an input, each inverter being coupled to a different terminal of a multi-terminal device under test, wherein said inverters receive a third voltage and a fourth voltage as power supplies,

wherein current drawn a first inverter of said inverters provides a measurement of capacitance of a first terminal of said multi-terminal device under test while remaining ones of said inverters isolate current drawn by said first inverter to only that associated with said first terminal,

~~The structure in claim 15~~, wherein a difference between said third and fourth voltages is less than or equal to approximately one-third of the difference between said first and second voltages.

17. (Currently Amended) The structure in claim [[15]] 16, wherein a difference between said third and fourth is less than the sum of absolute values of threshold voltages of n-type and p-type field effect transistors that comprise said inverter.

18. (Currently Amended) The structure in claim [[15]] 16, wherein said capacitance comprises:

said current drawn by said inverter divided by a multiplication result of the frequency of said ring oscillator output multiplied by the difference between said third and fourth voltages; less

a capacitance constant for said structure.

19. (Original) The structure in claim 18, wherein said capacitance constant is for said semiconductor structure alone and does not include any part of said capacitance of said device under test.

20. (Currently Amended) The structure in claim [[15]] 16, wherein said measurement of capacitance of said device under test is used to determine the thickness of a gate oxide.

21. (Original) The structure in claim 15, wherein said device under test comprises one of a gate oxide capacitor, a gate conductor, a channel, and an interconnect.

22. (Canceled).

23. A method of testing the capacitance of a device under test in an integrated circuit chip, said method comprising:

supplying an output of a ring oscillator to an inverter to produce an inverted ring oscillator output, wherein said inverter receives different voltages as power supplies; and

inputting said inverted ring oscillator output to said device under test,

determining current drawn by said inverter to provide a measurement of capacitance of said device under test,

~~The method in claim 22,~~ wherein said difference between said voltages is less than or equal to approximately one-third of the difference between a second set of voltages provided to said ring oscillator.

24. (Currently Amended) The method in claim [[22]] 23, wherein said difference between said voltages is less than the sum of absolute values of threshold voltages of n-type and p-type field effect transistors that comprise said inverter.

25. (Currently Amended) The method in claim [[22]] 23, further comprising calculating said capacitance by:

multiplying the frequency of said ring oscillator output by the difference between said voltages to produce a first result;

dividing said current drawn by said inverter by said first result to produce a second result; and

subtracting a capacitance constant for a testing device from said second result.

26. (Currently Amended) The method in claim [[22]] 23, wherein said capacitance constant is for said testing device alone and does not include any part of said capacitance of said device under test.

27. (Currently Amended) The method in claim [[22]] 23, wherein said device under test comprises a gate oxide capacitor.

28. (Original) The method in claim 27, wherein said measurement of capacitance of said device under test is used to determine the thickness of said gate oxide capacitor.

29. (Currently Amended) The method in claim [[22]] 23, wherein said device under test comprises one of a gate conductor, a channel, and an interconnect.